IN THE CLAIMS

The following listing of claims replaces all previous listings and versions of claim in this application:

1. (Currently amended) A method of preparing a semiconductor wafer, comprising:

growing a first layer of a first material in a strained state on a matching substrate comprising a matching layer;

growing a second layer of a semiconductor second material, different from the first material, in a relaxed state on the first layer to form a boundary between the first and second layers and to form a composite structure which comprises the matching, first, and second layers, wherein the first and second layers each have substantially the same first lattice parameter;

creating a region of weakness in the matching substrate to facilitate splitting;

splitting the composite structure at the region of weakness into:

an unfinished wafer that includes the second layer, the first layer, and at least a remaining portion of the matching layer, and

a handle wafer;

removing the remaining portion of the matching layer from the first layer; and

removing the first layer from the second layer to produce a surface on the second layer that is substantially smooth and of substantially uniform thickness.

2. (Cancelled)

3. (Original) The method of claim 1, wherein the matching layer has the lattice parameter where it contacts the first layer that is substantially the same as the first lattice parameter of the first layer.

4. (Original) The method of claim 1, further comprising growing the matching layer on a handling substrate that has a second lattice parameter that is different from the first lattice parameter.

5. (Original) The method of claim 1, wherein the matching layer includes a buffer layer and a relaxed surface layer.

6. (Original) The method of claim 5, wherein the lattice parameter of the matching layer is graded between the first and second lattice parameters.

7. (Original) The method of claim 6, wherein the region of weakness is created in a portion of the matching layer that is in a substantially relaxed state.

8-9. (Cancelled)

10. (Currently amended) The method of claim ~~8~~ 1, further comprising associating a receiving substrate with the second layer of the composite structure prior to splitting.

11. (Original) The method of claim 10, wherein the receiving substrate is bonded to the second layer.

12. (Currently amended) The method of claim ~~+~~ 10, further comprising providing an insulator between the second layer and receiving substrate.

13. (Original) The method of claim 1, wherein the region of weakness is created by implanting atomic species.

14. (Original) The method of claim 1, wherein the region of weakness is created by adding a porous layer.

15. (Original) The method of claim 1, wherein the first layer is strained to impart the first lattice parameter.

16. (Original) The method of claim 15, wherein the lattice parameter of the first material when strained is different than the lattice parameter of the first material in a relaxed state.

17. (Cancelled)

18. (Currently amended) The method of claim ~~17~~ 1, wherein the first layer is removed by etching.

19. (Cancelled)

20. (Original) The method of claim 1, wherein the boundary with the first layer removed is sufficiently smooth for growing a substantially uniform and substantially smooth device layer thereon of a semiconductor material that is different from that of the second layer and that has a lattice parameter that is adapted to match that of the second layer.

21. (Original) The method of claim 1, wherein the first material is a semiconductor.

22. (Previously presented) The method of claim 1, further comprising growing a device layer on the surface.

23. (Original) The method of claim 1, wherein the region of weakness is created at a depth from the second layer sufficient for substantially preventing damage to the second layer.

24. (Original) The method of claim 23, wherein a damaged region in the matching substrate and outside the second layer is created adjacent the region of weakness by the creation of the region of weakness.

25. (Original) The method of claim 1, wherein the matching layer and the second layer comprise silicon germanium.

26-35. (Cancelled)

36. (Previously presented) The method of claim 1, wherein the produced surface of the second layer is substantially at said boundary.

37. (Previously presented) The method of claim 18, wherein the remaining portion of the matching layer is removed from the unfinished wafer by etching.

38. (Previously presented) The method of claim 23, wherein the region of weakness is created by implanting atomic species to said depth.

39. (Previously presented) The method of claim 23, wherein the first layer is removed by selective etching.

40. (New) The method of claim 1, wherein the remaining portion of the matching layer is removed from the first layer and the first layer are removed from the second layer by selective removal processes.

41. (New) The method of claim 40, wherein the selective removal processes each comprises selective etching.

42. (New) A method of preparing a semiconductor wafer, comprising:

providing a first layer of material in a strained state on a matching substrate that comprises a matching layer;

growing a second layer of a semiconductor second material, different from the first material, in a relaxed state on the first layer to form a boundary between the first and second layers and to form a composite structure which comprises the matching, first, and second layers, wherein the first and second layers each have substantially the same first lattice parameter;

creating a region of weakness in the matching substrate to facilitate splitting;

splitting the composite structure into:

an unfinished wafer that includes the second layer and at least a remaining portion of the matching layer, and

a handle wafer;

removing the remaining portion of the matching layer from the unfinished wafer by selective etching; and

removing the first layer from the second layer by selective etching to produce a surface on the second layer.